

## METHOD FOR IMPROVED FIRST LEVEL CACHE COHERENCY

### ABSTRACT OF THE DISCLOSURE

5           A method of and apparatus for improving the efficiency of a  
data processing system employing a multiple level cache memory  
system. The efficiencies result from invalidating level one cache  
information based upon a level one cache memory write. Similarly,  
the invalidation can occur from system bus SNOOPs. In addition,  
10           level one and level two cache memory misses result in loading and  
recording of the requested<sub>1</sub> into both level one and level two cache  
memories. Furthermore, a level two cache memory parity error  
results in invalidation of the corresponding level one cache memory  
data.